REMARKS

The application is believed in condition for allowance for the reasons set forth below.

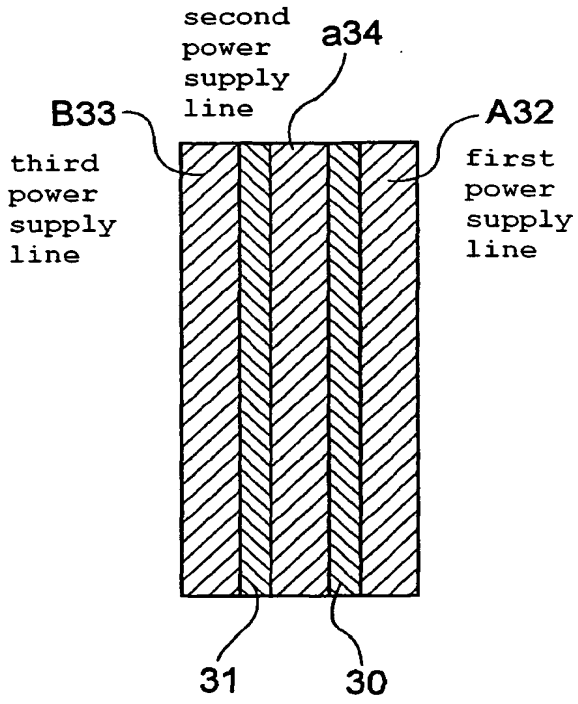
Claims 2-6, 8, 16-23, 31 and 32 are pending in the application. Claims 5, 8 and 16-23 are withdrawn from consideration as being directed to a non-elected species.

Claims 2, 4, 31 and 32 were rejected over applicant's disclosed prior art in view of IRANMANESH et al. (6,177,691) or Chinese Patent (CN1239355). That rejection is respectfully traversed.

Independent claim 31 recites that first, second and third power supply lines are arranged side by side in that order. Claim 31 also recites that a first transistor switches between the first and second power supply lines and a second transistor switches between the second and third power supply lines. An embodiment of the present invention that meets these limitations is shown with respect to Figures 1 and 4, reproduced below.

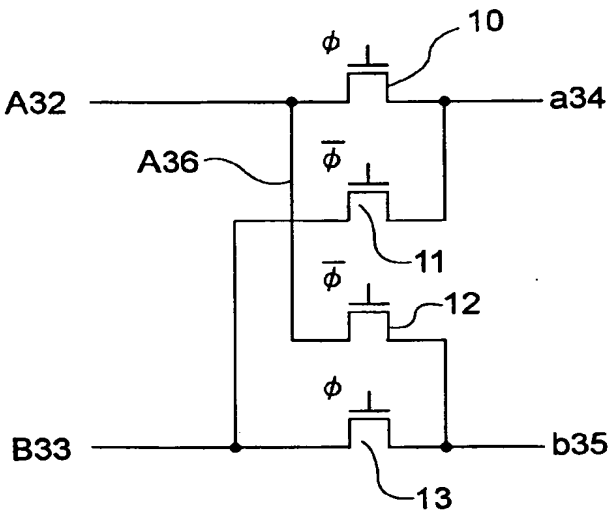
As seen from Figure 1, power supply lines A32, a34 and B33 are arranged in that order as first, second and third power supply lines.

FIG. 1



As seen in Figure 4, transistor 10 (first transistor) is between the first and second power supply lines (A32 and a34) and switches the first and second power supply lines (A32 and a34). Transistor 11 (second transistor) is between second and third power supply lines (a34 and B33) and switches the second and third power supply lines (a34 and B33).

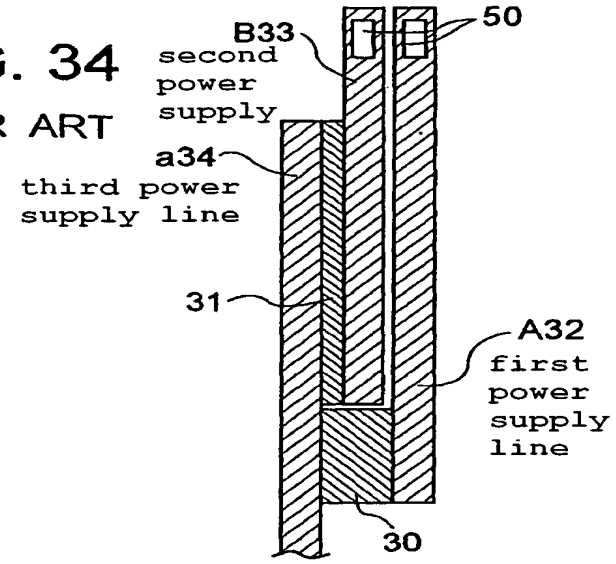
FIG. 4



WIRING SWITCH CIRCUIT

In applicant's disclosed prior art Figures 2 and 34, reproduced below, if the power supply lines are arranged as first, second and third power supply lines in that order (as recited), then A32 would be the first power supply line, B33 would be the second power supply line and a34 would be the third power supply line as seen in the marked-up version of Figure 34.

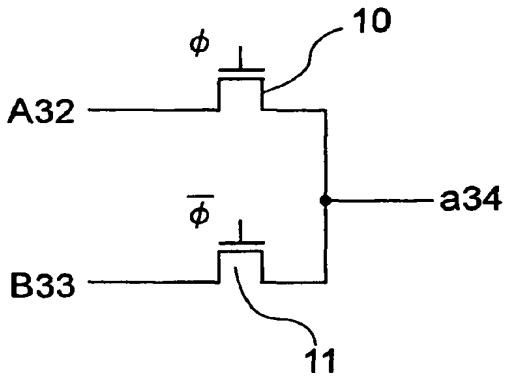
FIG. 34
PRIOR ART



EXAMPLE OF ORDINARY LAYOUT

However, using the above arrangement of power supply lines (as required to meet the first limitation of the claim), the transistor arrangement of Figure 2 would not meet the recited limitation as suggested in the Official Action.

FIG. 2



WIRING SWITCH CIRCUIT

As seen in Figure 2, the second transistor (11) is between (and switches between) the second and third power supply lines (B33 and a34). However, the first transistor (10) is between (and switches between) the first and third power supply lines (A32 and a34), not between the first and second power supply lines as recited. Even assigning different labels to the power supply lines of prior art Figures 2 and 34, the transistor arrangement of these figures would not meet the limitations of claim 31.

Neither IRANMANESH nor the Chinese reference overcomes the shortcomings of Applicant's disclosed prior art.

Rather, IRANMANESH teaches an arrangement of power supply lines that are in a different order than that which is recited. In addition, IRANMANESH teaches a different function of the switching of the power lines by the transistors than that of the present invention.

Specifically, Figures 1 and 7 of IRANMANESH shows three power lines, such as VSS(1), VDD and VSS(2) and two transistors, such as transistors 70 and 125 arranged in the order of VSS(1), VDD, transistor 70, transistor 125 and VSS(2).

On the other hand, in order to meet the limitations of claim 31, the power lines and transistors would have to be arranged as follows: VSS(1), transistor 70, VDD, transistor 125 and VSS(2).

Thus, not only is the arrangement of the power supply lines and transistors different that that which is recited, but the control method of transistor 70 switching VSS(1) and VDD, and transistor 125 switching between VDD and VSS(2) cannot be obtained from the arrangement of IRANMANESH.

The Chinese reference does not disclose an arrange,ent or layout of transistors and power supply lines and thus could not meet the limitations of claim 31.

Accordingly, the secondary references do not appear particularly relevant to the recited powerline/transistor configuration and applicant respectfully requests that the Examiner contact the below named attorney to further discuss these references, if the above remarks do place the application in condition for allowance.

Claim 3 was rejected over applicant's disclosed prior art in view of IRANMANESH et al. or the Chinese Patent and further in view of FUJII et al. (6,707,139). That rejection is respectfully traversed.

FUJII is only cited for the teaching of a mutual connection line for connecting power supply lines having equal potentials. FUJII does not teach or suggest what is recited in claim 31. As set forth above, applicant's disclosed prior art in view of IRANMANESH or the Chinese Patent does not teach or suggest what is recited in claim 31. Since claim 3 depends from claim 31 and further defines the invention, the proposed

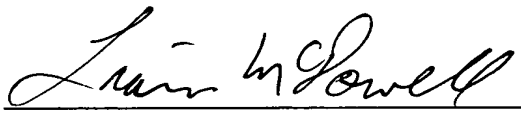
combination of references would not have rendered obvious claim 3.

In view of the foregoing remarks, it is believed that the present application is in condition for allowance. Reconsideration and allowance are respectfully requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

YOUNG & THOMPSON



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